Electronic Version
Stylesheet Version v1.1.1

[AUTONOMIC GRAPHICAL PARTITION-ING]

Abstract

Disclosed is a method and structure that partitions an integrated circuit design by identifying logical blocks within the integrated circuit design based on size heuristics of logical macros in the design hierarchy. The invention determines whether the number of logical blocks is within a range of desired number of logical blocks and repeats the process of identifying logical blocks for different hierarchical levels of the integrated circuit design until the number of logical blocks is within the range of the desired number of logical blocks. This serves as a guide to partition the chip as opposed to a grid-like partitioning.